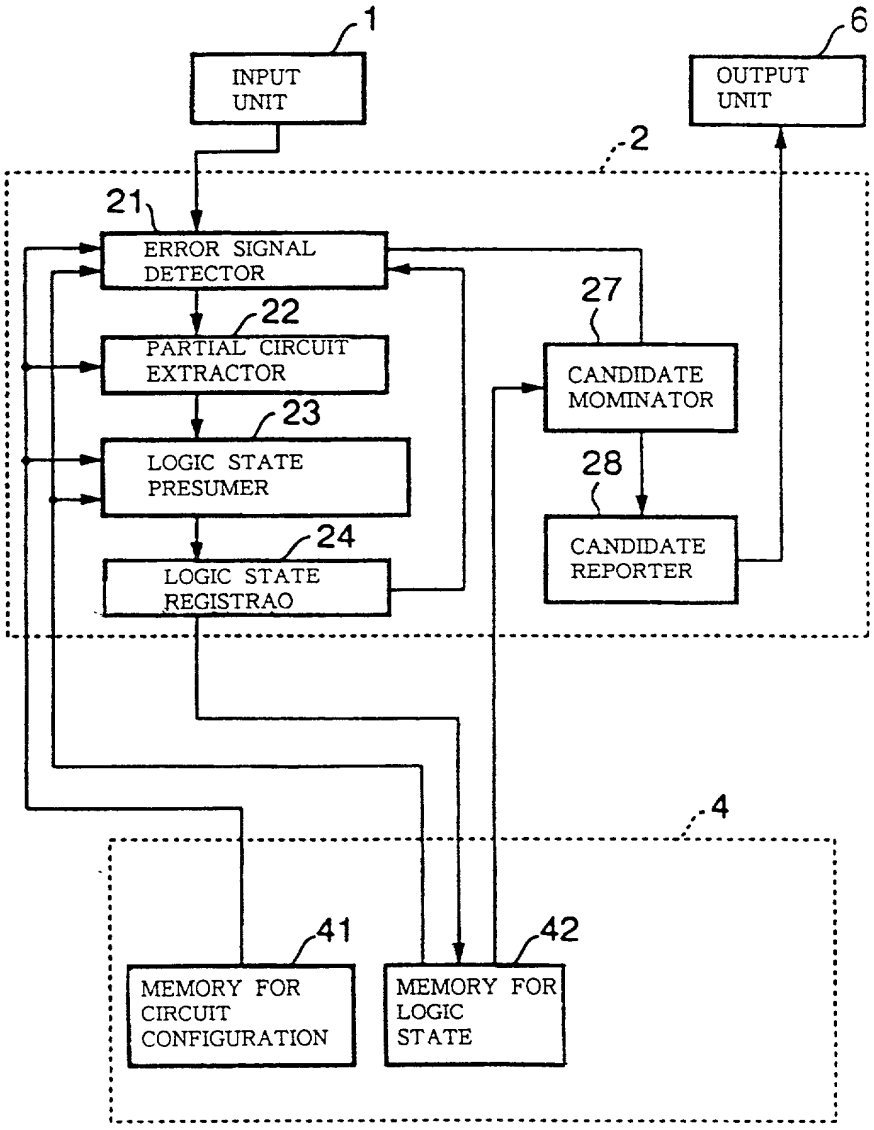

Fig. 1
PRIOR ART

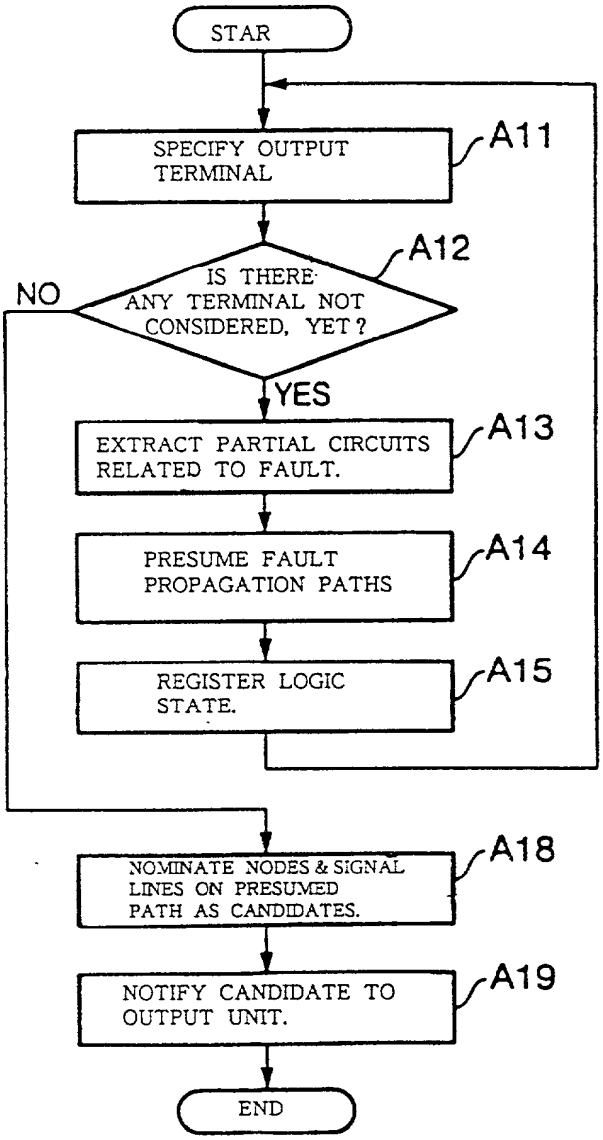

Fig. 2
PRIOR ART

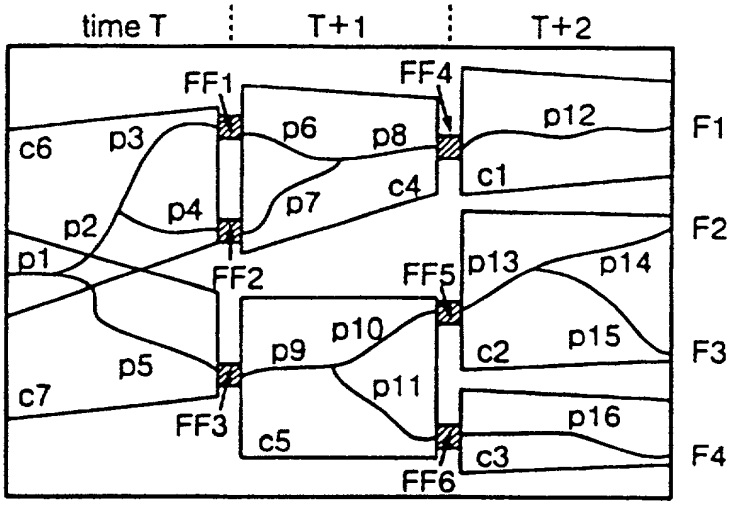

Fig. 3
PRIOR ART

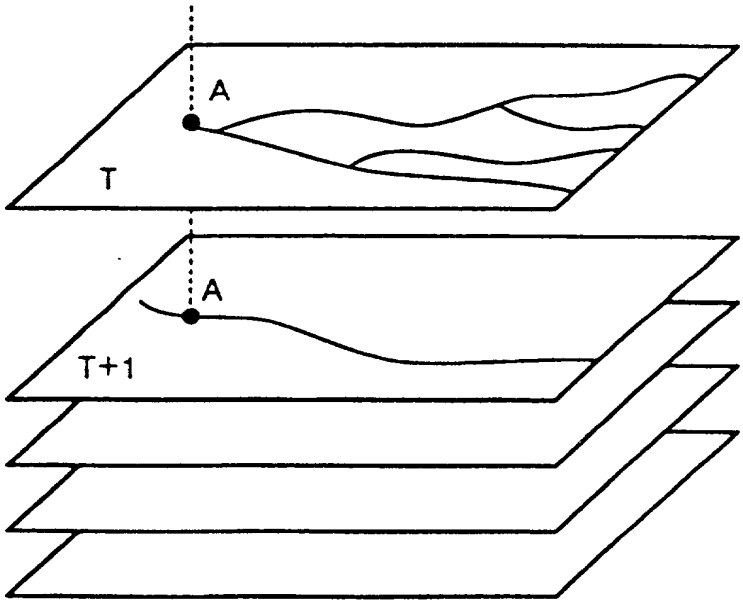

Fig. 15

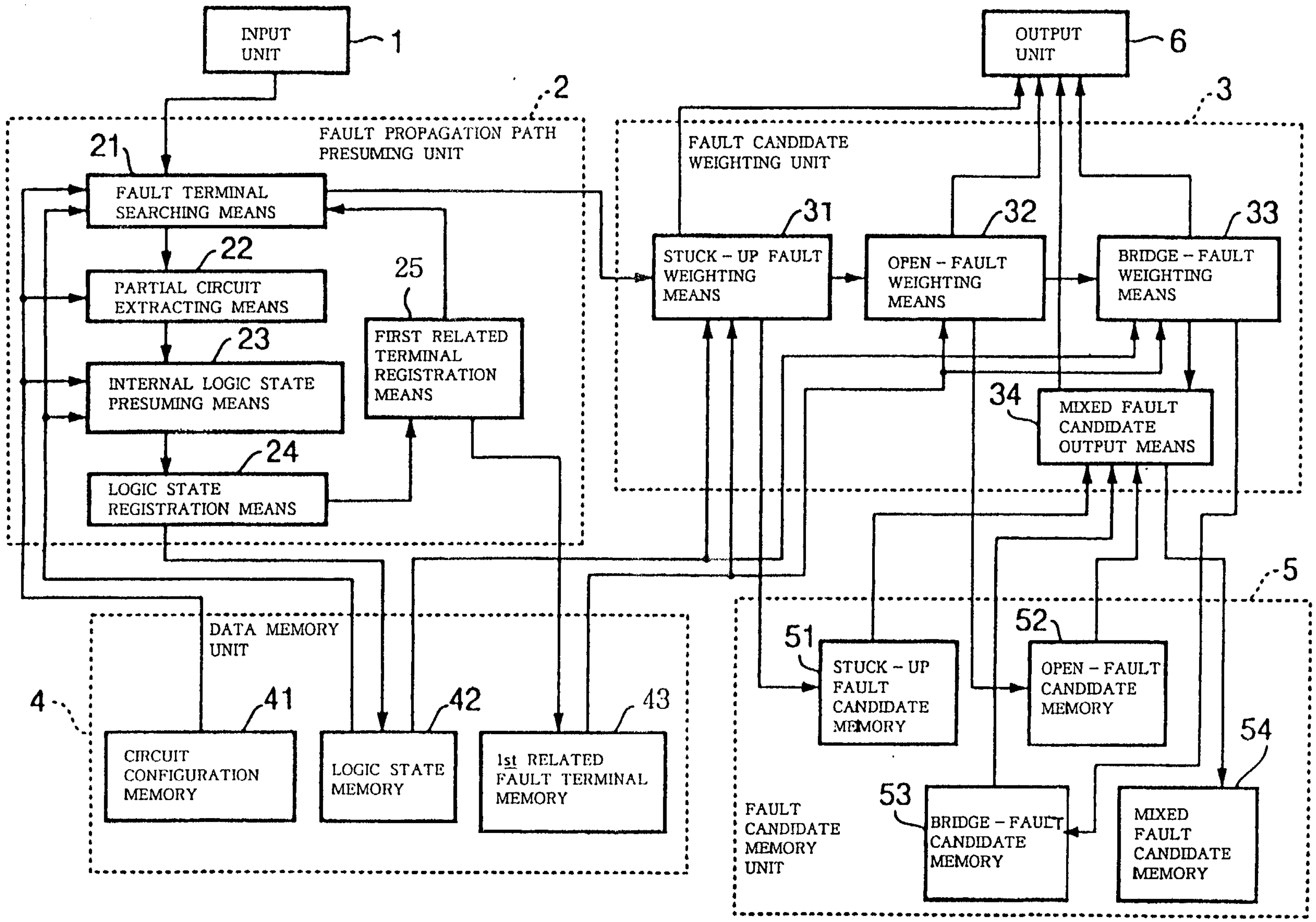
INPUT UNIT
1
OUTPUT UNIT
6
2
FAULT PROPAGATION PATH PRESUMING UNIT
3
FAULT CANDIDATE WEIGHTING UNIT
21
FAULT TERMINAL SEARCHING MEANS
22
PARTIAL CIRCUIT EXTRACTING MEANS
23
INTERNAL LOGIC STATE PRESUMING MEANS
24
LOGIC STATE REGISTRATION MEANS
25
FIRST RELATED TERMINAL REGISTRATION MEANS
31
STUCK – UP FAULT WEIGHTING MEANS
32
OPEN – FAULT WEIGHTING MEANS
33
BRIDGE – FAULT WEIGHTING MEANS
34
MIXED FAULT CANDIDATE OUTPUT MEANS
4
DATA MEMORY UNIT
41
CIRCUIT CONFIGURATION MEMORY
42
LOGIC STATE MEMORY
43
1st RELATED FAULT TERMINAL MEMORY
5
FAULT CANDIDATE MEMORY UNIT
51
STUCK – UP FAULT CANDIDATE MEMORY
52
OPEN – FAULT CANDIDATE MEMORY
53
BRIDGE – FAULT CANDIDATE MEMORY
54
MIXED FAULT CANDIDATE MEMORY

Fig. 4

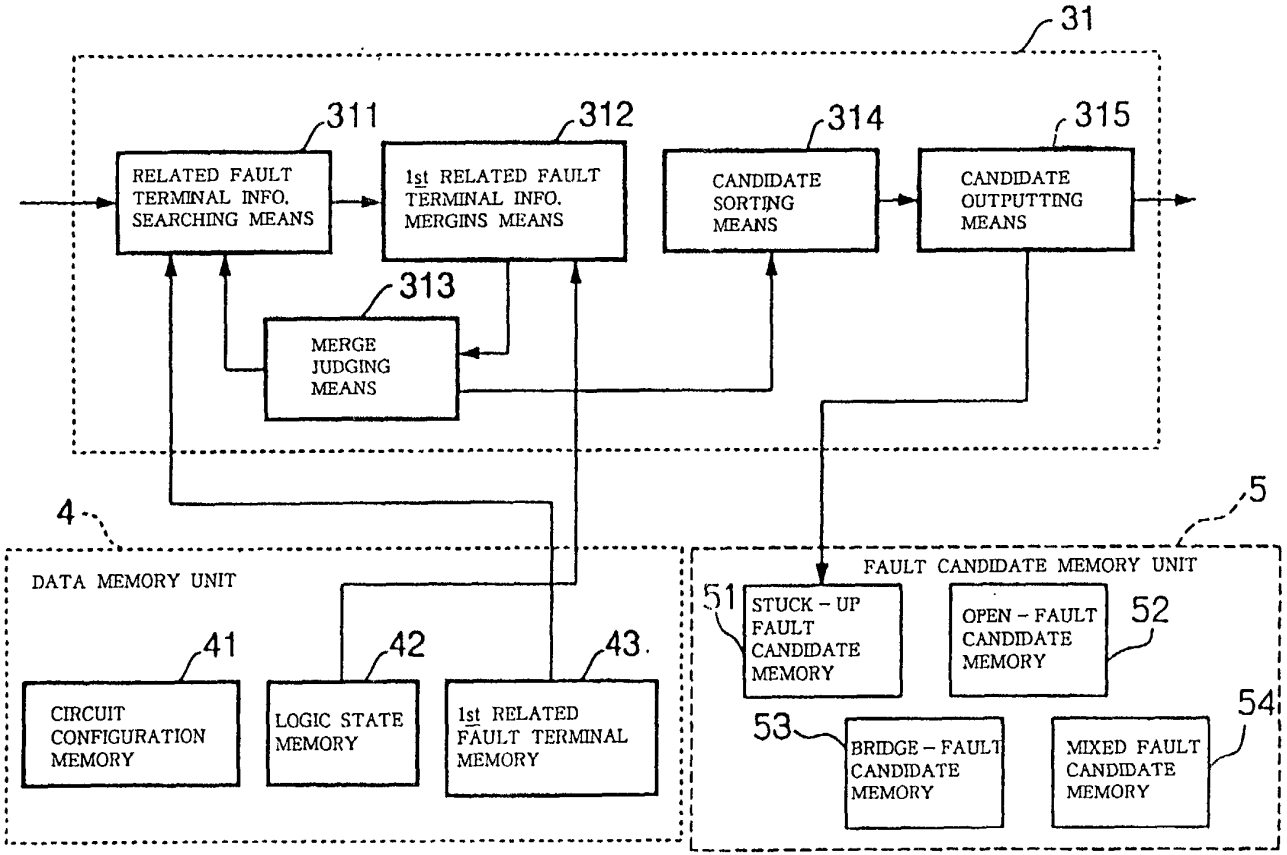
31
311
RELATED FAULT TERMINAL INFO. SEARCHING MEANS
312
1st RELATED FAULT TERMINAL INFO. MERGINS MEANS
314
CANDIDATE SORTING MEANS
315
CANDIDATE OUTPUTTING MEANS
313
MERGE JUDGING MEANS
4
DATA MEMORY UNIT
41
CIRCUIT CONFIGURATION MEMORY
42
LOGIC STATE MEMORY
43
1st RELATED FAULT TERMINAL MEMORY
5
FAULT CANDIDATE MEMORY UNIT
51
STUCK – UP FAULT CANDIDATE MEMORY
52
OPEN – FAULT CANDIDATE MEMORY
53
BRIDGE – FAULT CANDIDATE MEMORY
54
MIXED FAULT CANDIDATE MEMORY

Fig. 5

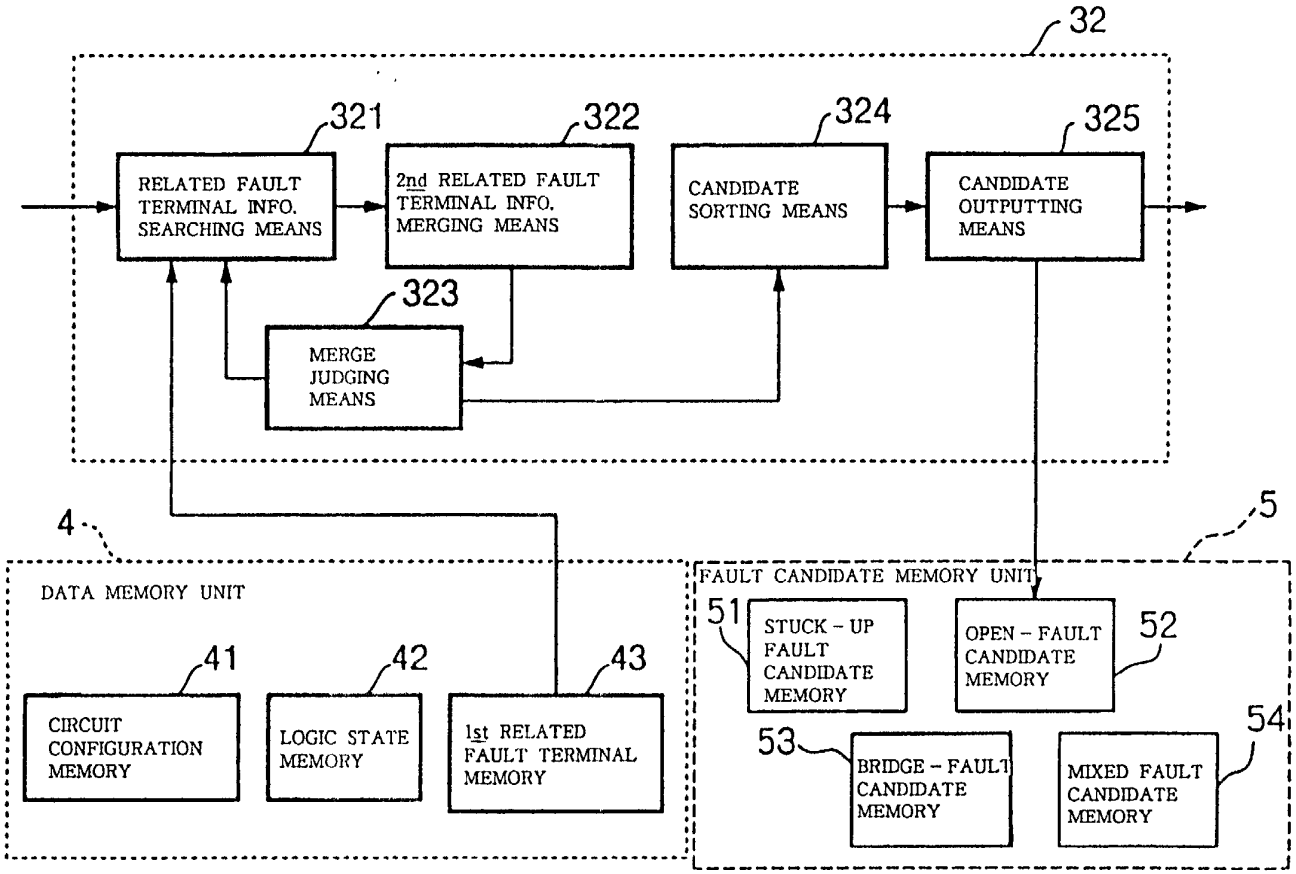
32
321
322
324
325
RELATED FAULT TERMINAL INFO. SEARCHING MEANS
2nd RELATED FAULT TERMINAL INFO. MERGING MEANS
CANDIDATE SORTING MEANS
CANDIDATE OUTPUTTING MEANS
323
MERGE JUDGING MEANS
4
5
DATA MEMORY UNIT
FAULT CANDIDATE MEMORY UNIT
41
42
43
CIRCUIT CONFIGURATION MEMORY
LOGIC STATE MEMORY
1st RELATED FAULT TERMINAL MEMORY
51
STUCK - UP FAULT CANDIDATE MEMORY
OPEN - FAULT CANDIDATE MEMORY
52
53
BRIDGE - FAULT CANDIDATE MEMORY
MIXED FAULT CANDIDATE MEMORY
54

Fig. 6

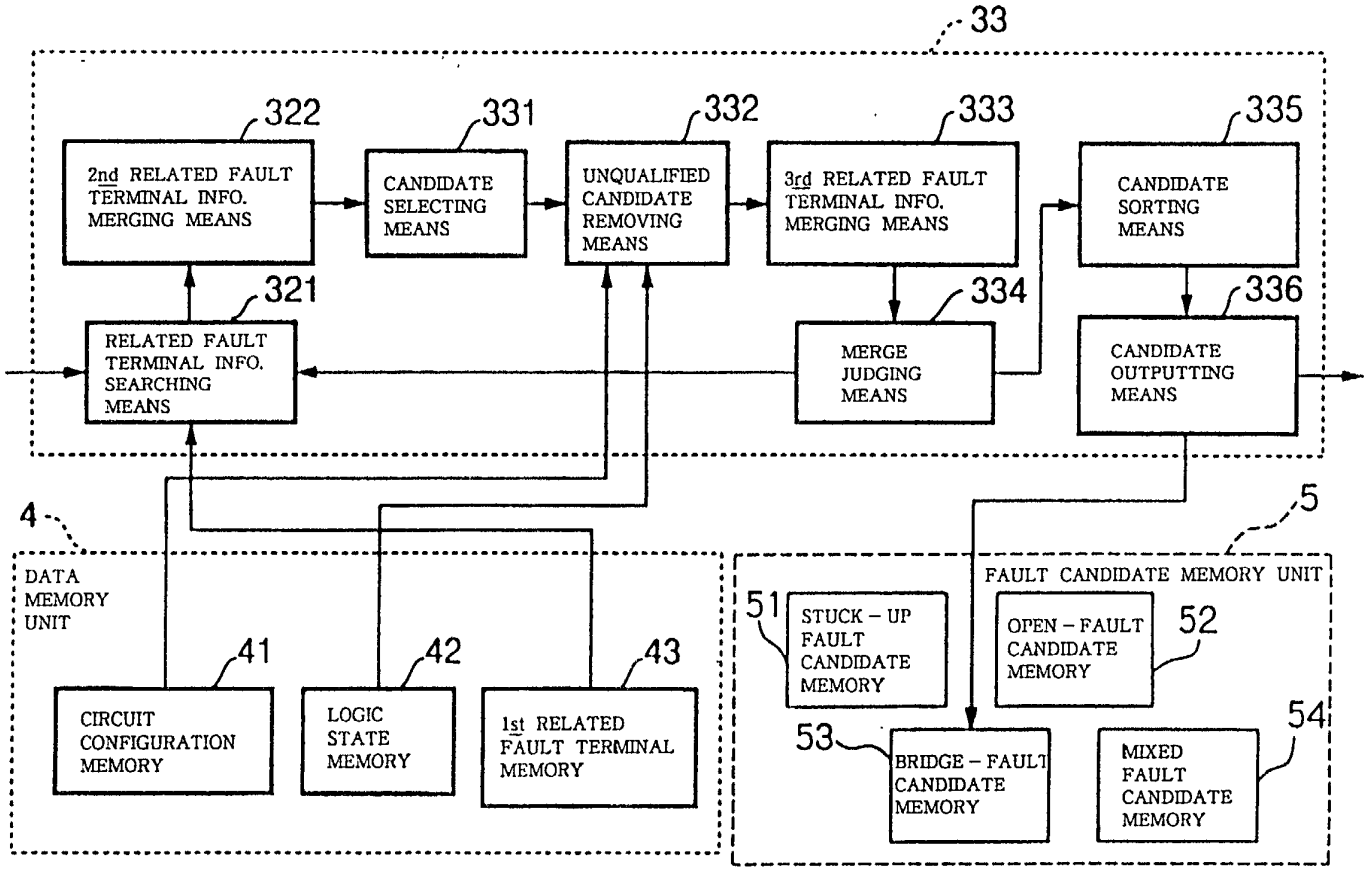
33
322
2nd RELATED FAULT TERMINAL INFO. MERGING MEANS
331
CANDIDATE SELECTING MEANS
332
UNQUALIFIED CANDIDATE REMOVING MEANS
333
3rd RELATED FAULT TERMINAL INFO. MERGING MEANS
335
CANDIDATE SORTING MEANS
321
RELATED FAULT TERMINAL INFO. SEARCHING MEANS
334
MERGE JUDGING MEANS
336
CANDIDATE OUTPUTTING MEANS
4
DATA MEMORY UNIT
41
CIRCUIT CONFIGURATION MEMORY
42
LOGIC STATE MEMORY
43
1st RELATED FAULT TERMINAL MEMORY
5
FAULT CANDIDATE MEMORY UNIT
51
STUCK – UP FAULT CANDIDATE MEMORY
52
OPEN – FAULT CANDIDATE MEMORY
53
BRIDGE – FAULT CANDIDATE MEMORY
54
MIXED FAULT CANDIDATE MEMORY

Fig. 7

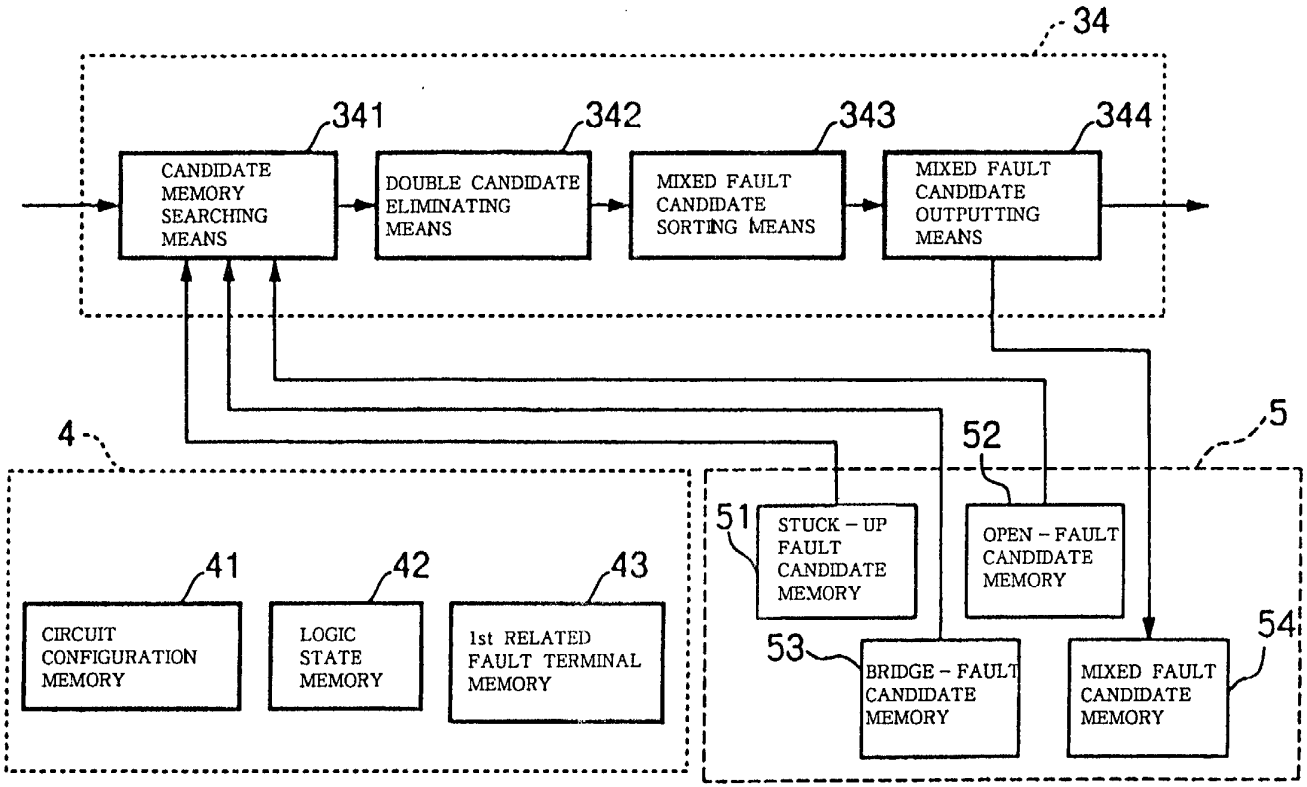
34
341
342
343
344
CANDIDATE MEMORY SEARCHING MEANS
DOUBLE CANDIDATE ELIMINATING MEANS
MIXED FAULT CANDIDATE SORTING MEANS
MIXED FAULT CANDIDATE OUTPUTTING MEANS
4
5
52
51
STUCK – UP FAULT CANDIDATE MEMORY
OPEN – FAULT CANDIDATE MEMORY
41
42
43
CIRCUIT CONFIGURATION MEMORY
LOGIC STATE MEMORY
1st RELATED FAULT TERMINAL MEMORY
53
54
BRIDGE – FAULT CANDIDATE MEMORY
MIXED FAULT CANDIDATE MEMORY

Fig. 8

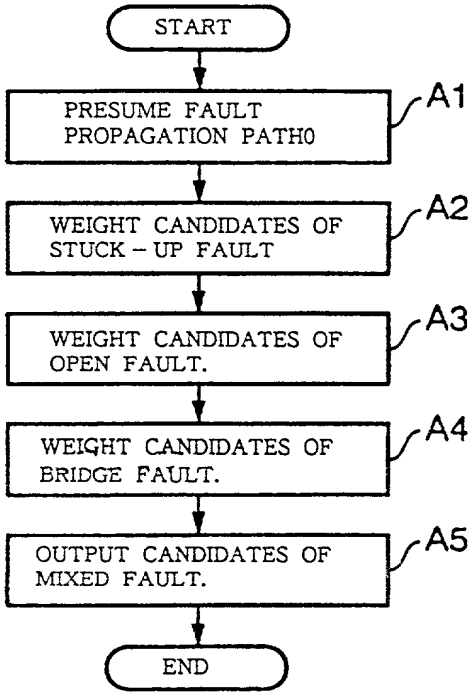
START
PRESUME FAULT PROPAGATION PATH0
A1
WEIGHT CANDIDATES OF STUCK – UP FAULT
A2
WEIGHT CANDIDATES OF OPEN FAULT.
A3
WEIGHT CANDIDATES OF BRIDGE FAULT.
A4
OUTPUT CANDIDATES OF MIXED FAULT.
A5
END

Fig. 9

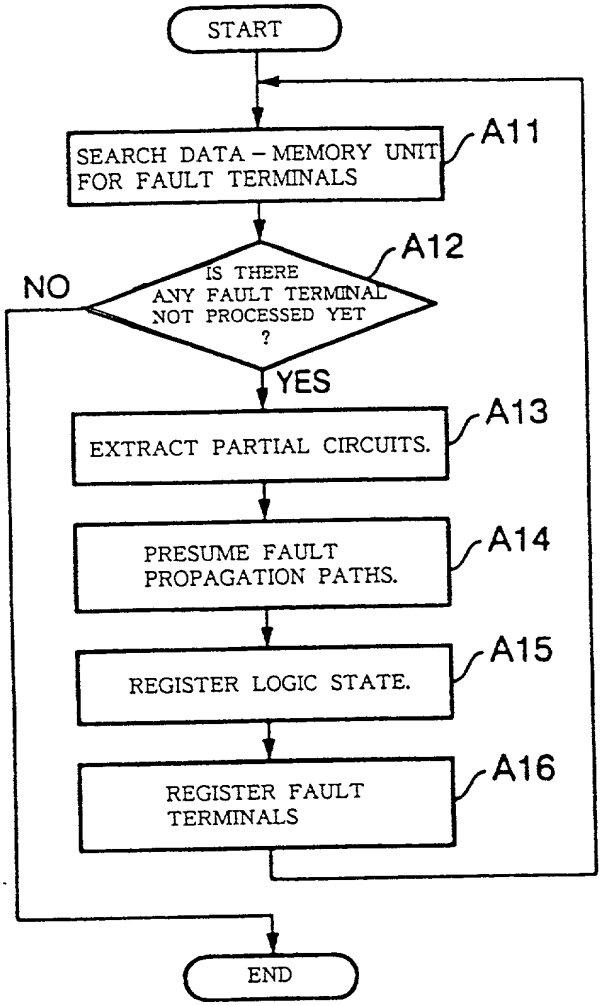
START
SEARCH DATA – MEMORY UNIT FOR FAULT TERMINALS
A11
IS THERE ANY FAULT TERMINAL NOT PROCESSED YET ?
A12
NO
YES
EXTRACT PARTIAL CIRCUITS.
A13
PRESUME FAULT PROPAGATION PATHS.
A14
REGISTER LOGIC STATE.
A15
REGISTER FAULT TERMINALS
A16
END

Fig. 10

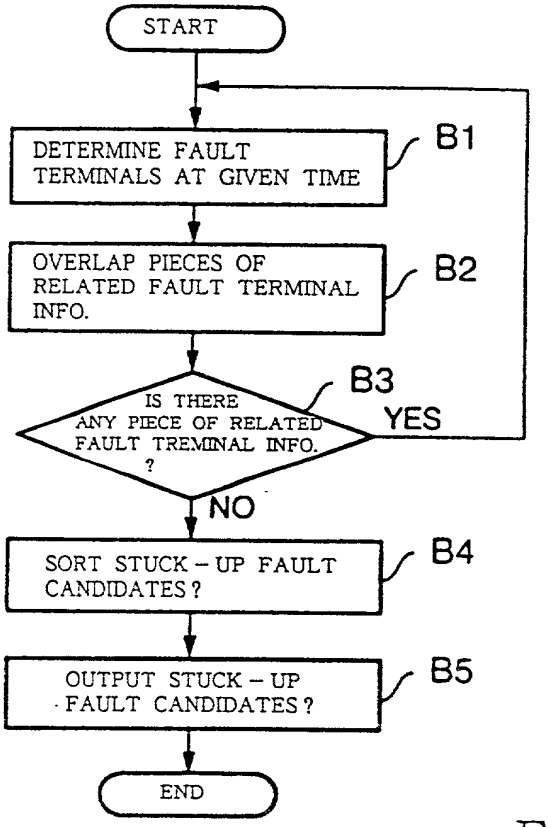
START
DETERMINE FAULT TERMINALS AT GIVEN TIME
B1
OVERLAP PIECES OF RELATED FAULT TERMINAL INFO.
B2
IS THERE ANY PIECE OF RELATED FAULT TREMINAL INFO. ?
B3
YES
NO
SORT STUCK – UP FAULT CANDIDATES ?
B4
OUTPUT STUCK – UP FAULT CANDIDATES ?
B5
END

Fig. 11

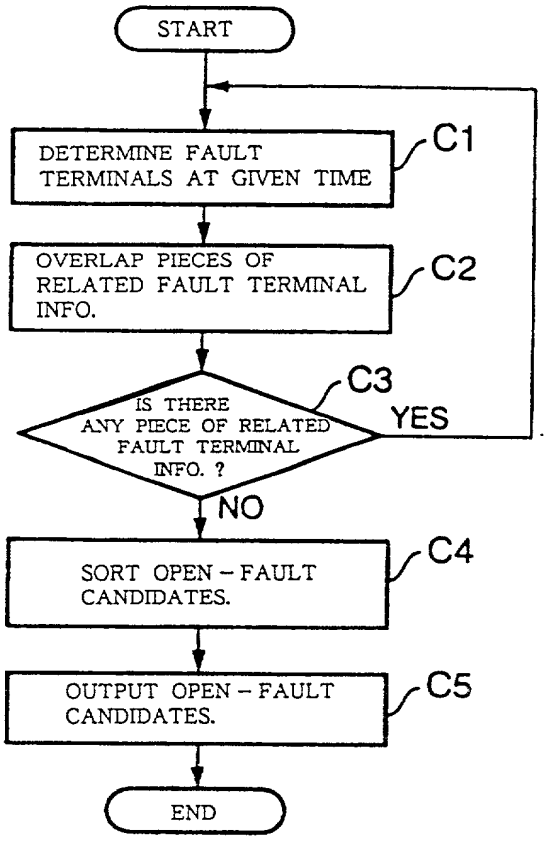
START
DETERMINE FAULT TERMINALS AT GIVEN TIME
C1
OVERLAP PIECES OF RELATED FAULT TERMINAL INFO.
C2
IS THERE ANY PIECE OF RELATED FAULT TERMINAL INFO. ?
C3
YES
NO
SORT OPEN – FAULT CANDIDATES.
C4
OUTPUT OPEN – FAULT CANDIDATES.
C5
END

Fig. 12

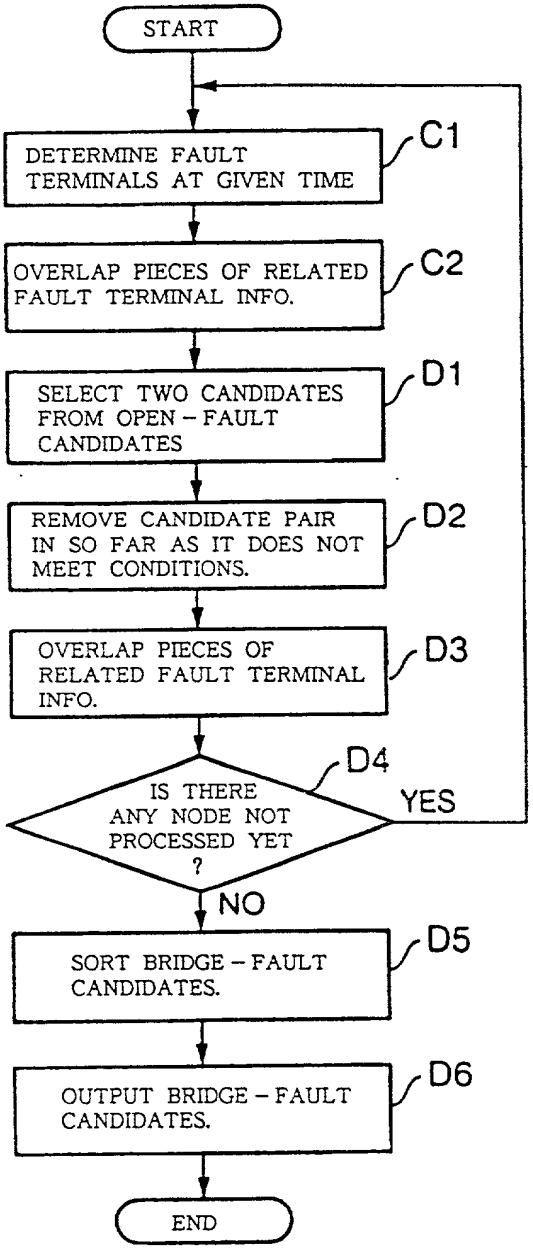
START
DETERMINE FAULT TERMINALS AT GIVEN TIME
C1
OVERLAP PIECES OF RELATED FAULT TERMINAL INFO.
C2
SELECT TWO CANDIDATES FROM OPEN – FAULT CANDIDATES
D1
REMOVE CANDIDATE PAIR IN SO FAR AS IT DOES NOT MEET CONDITIONS.
D2
OVERLAP PIECES OF RELATED FAULT TERMINAL INFO.
D3
IS THERE ANY NODE NOT PROCESSED YET ?
D4
YES
NO
SORT BRIDGE – FAULT CANDIDATES.
D5
OUTPUT BRIDGE – FAULT CANDIDATES.
D6
END

Fig. 13

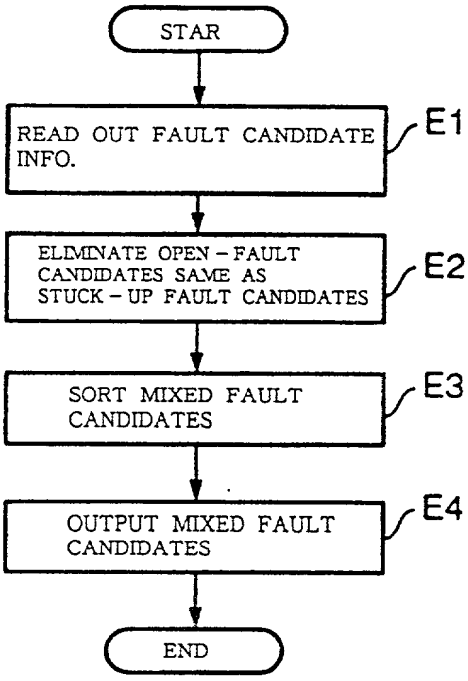
STAR
READ OUT FAULT CANDIDATE INFO.
E1
ELIMINATE OPEN - FAULT CANDIDATES SAME AS STUCK - UP FAULT CANDIDATES
E2
SORT MIXED FAULT CANDIDATES
E3
OUTPUT MIXED FAULT CANDIDATES
E4
END

Fig. 14

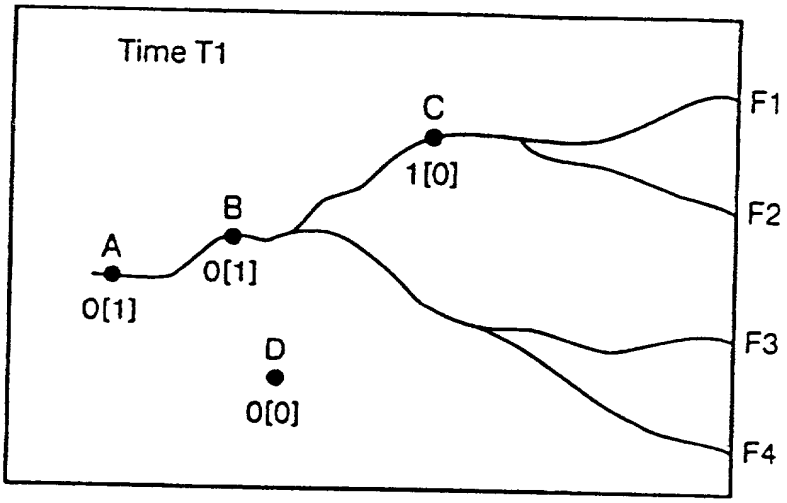

Fig. 16

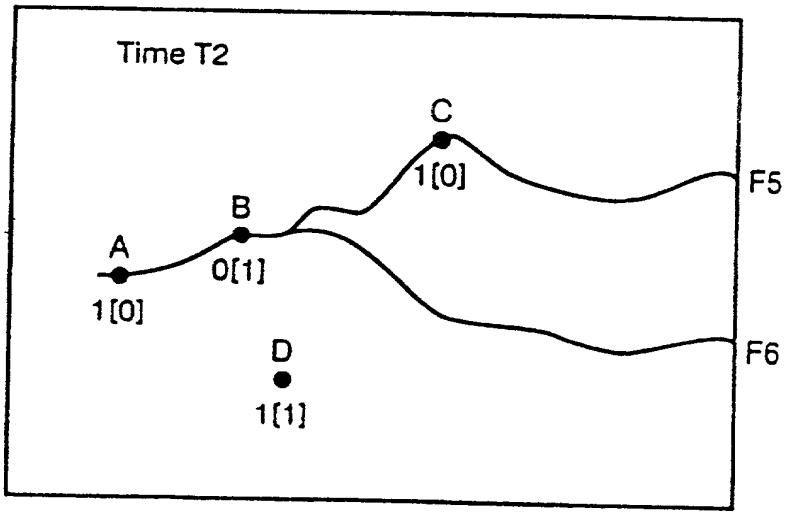

Fig. 17

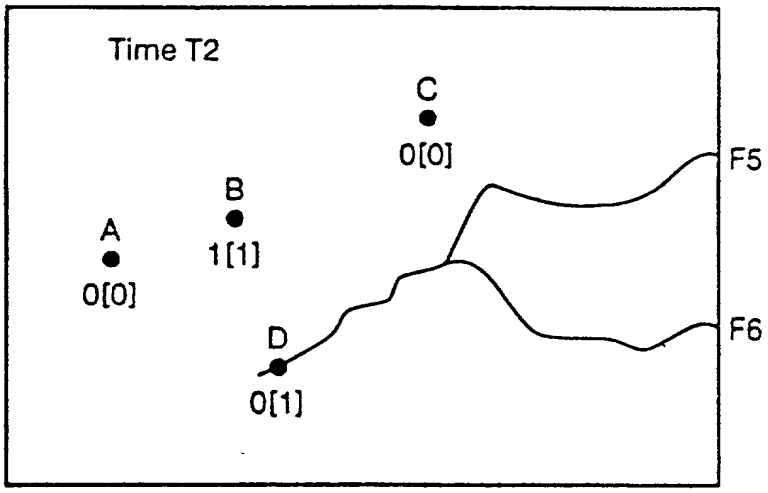

Fig. 18

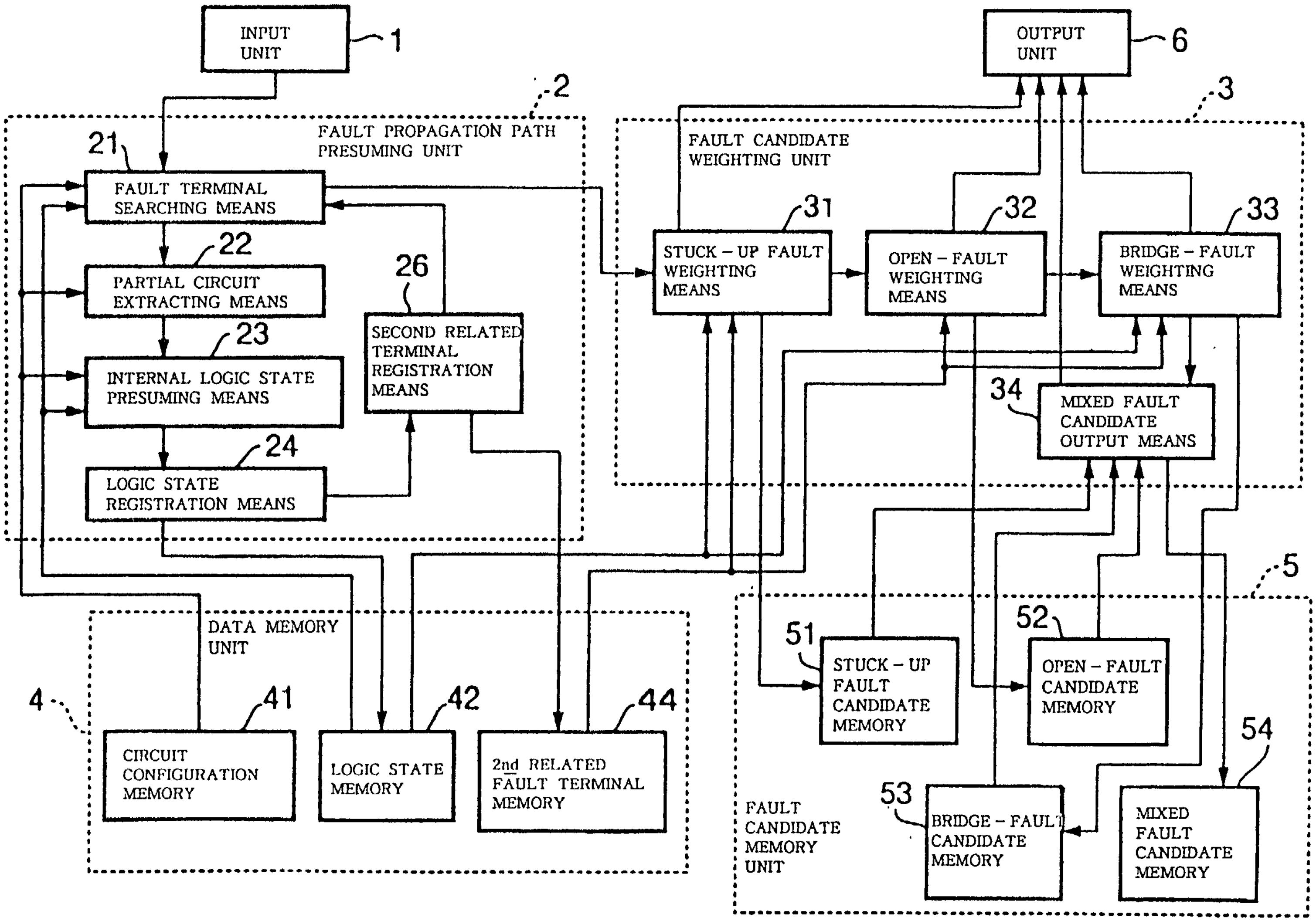
INPUT UNIT
1
FAULT PROPAGATION PATH PRESUMING UNIT
2
21
FAULT TERMINAL SEARCHING MEANS
22
PARTIAL CIRCUIT EXTRACTING MEANS
23
INTERNAL LOGIC STATE PRESUMING MEANS
24
LOGIC STATE REGISTRATION MEANS
26
SECOND RELATED TERMINAL REGISTRATION MEANS
OUTPUT UNIT
6
FAULT CANDIDATE WEIGHTING UNIT
3
31
STUCK – UP FAULT WEIGHTING MEANS
32
OPEN – FAULT WEIGHTING MEANS
33
BRIDGE – FAULT WEIGHTING MEANS
34
MIXED FAULT CANDIDATE OUTPUT MEANS
DATA MEMORY UNIT
4
41
CIRCUIT CONFIGURATION MEMORY
42
LOGIC STATE MEMORY
44
2nd RELATED FAULT TERMINAL MEMORY
5
FAULT CANDIDATE MEMORY UNIT
51
STUCK – UP FAULT CANDIDATE MEMORY
52
OPEN – FAULT CANDIDATE MEMORY
53
BRIDGE – FAULT CANDIDATE MEMORY
54
MIXED FAULT CANDIDATE MEMORY

Fig. 19

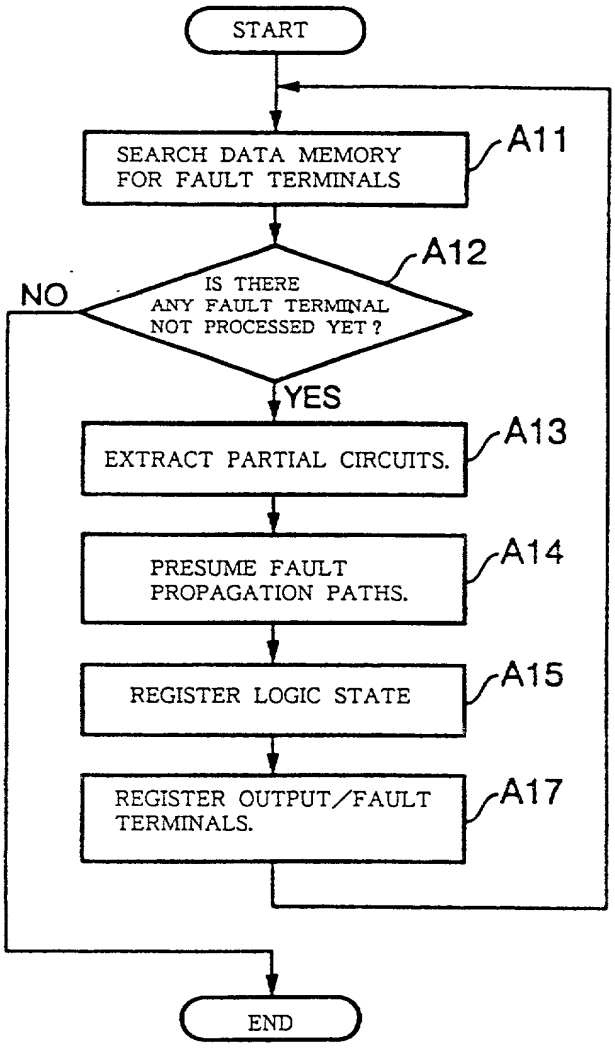
START
SEARCH DATA MEMORY FOR FAULT TERMINALS
A11
IS THERE ANY FAULT TERMINAL NOT PROCESSED YET ?
A12
NO
YES
EXTRACT PARTIAL CIRCUITS.
A13
PRESUME FAULT PROPAGATION PATHS.
A14
REGISTER LOGIC STATE
A15
REGISTER OUTPUT/FAULT TERMINALS.
A17
END

Fig. 20

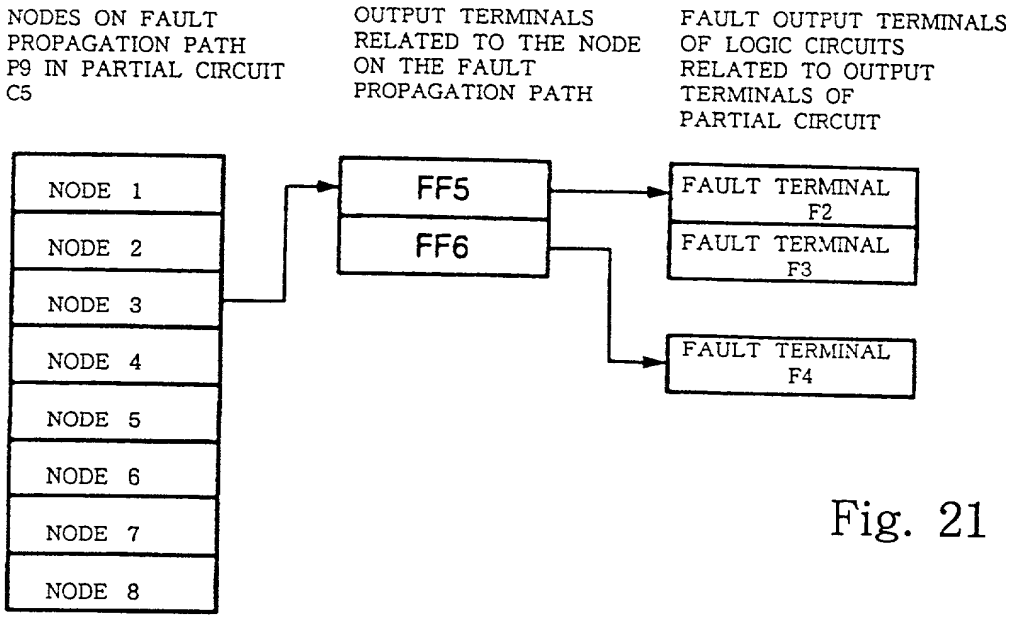
NODES ON FAULT PROPAGATION PATH P9 IN PARTIAL CIRCUIT C5
OUTPUT TERMINALS RELATED TO THE NODE ON THE FAULT PROPAGATION PATH
FAULT OUTPUT TERMINALS OF LOGIC CIRCUITS RELATED TO OUTPUT TERMINALS OF PARTIAL CIRCUIT
NODE 1
NODE 2
NODE 3
NODE 4
NODE 5
NODE 6
NODE 7
NODE 8
FF5
FF6
FAULT TERMINAL F2
FAULT TERMINAL F3
FAULT TERMINAL F4

Fig. 21

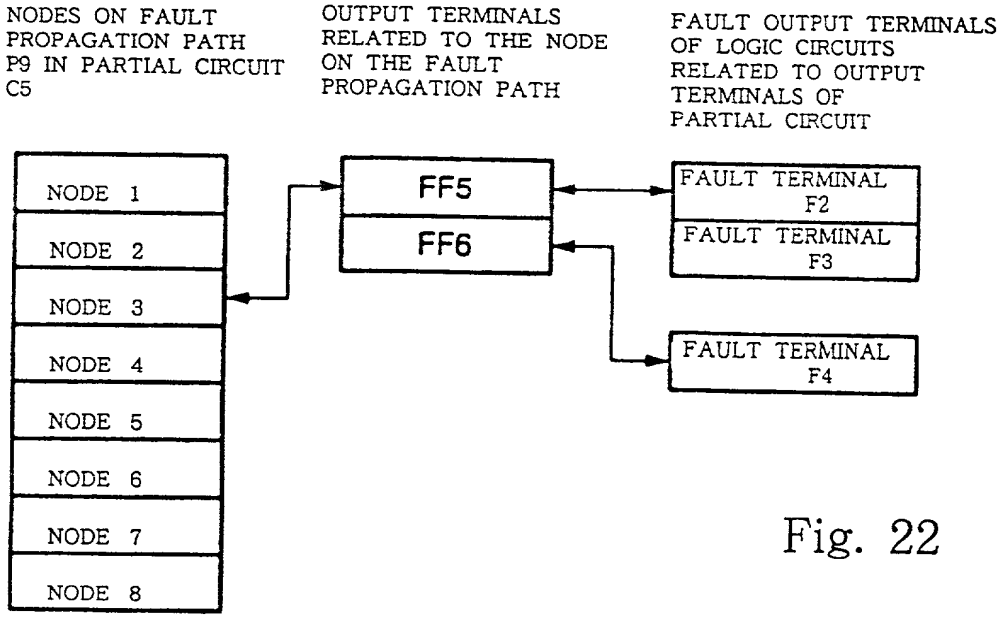
NODES ON FAULT PROPAGATION PATH P9 IN PARTIAL CIRCUIT C5
OUTPUT TERMINALS RELATED TO THE NODE ON THE FAULT PROPAGATION PATH
FAULT OUTPUT TERMINALS OF LOGIC CIRCUITS RELATED TO OUTPUT TERMINALS OF PARTIAL CIRCUIT
NODE 1
NODE 2
NODE 3
NODE 4
NODE 5
NODE 6
NODE 7
NODE 8
FF5
FF6
FAULT TERMINAL F2
FAULT TERMINAL F3
FAULT TERMINAL F4

Fig. 22

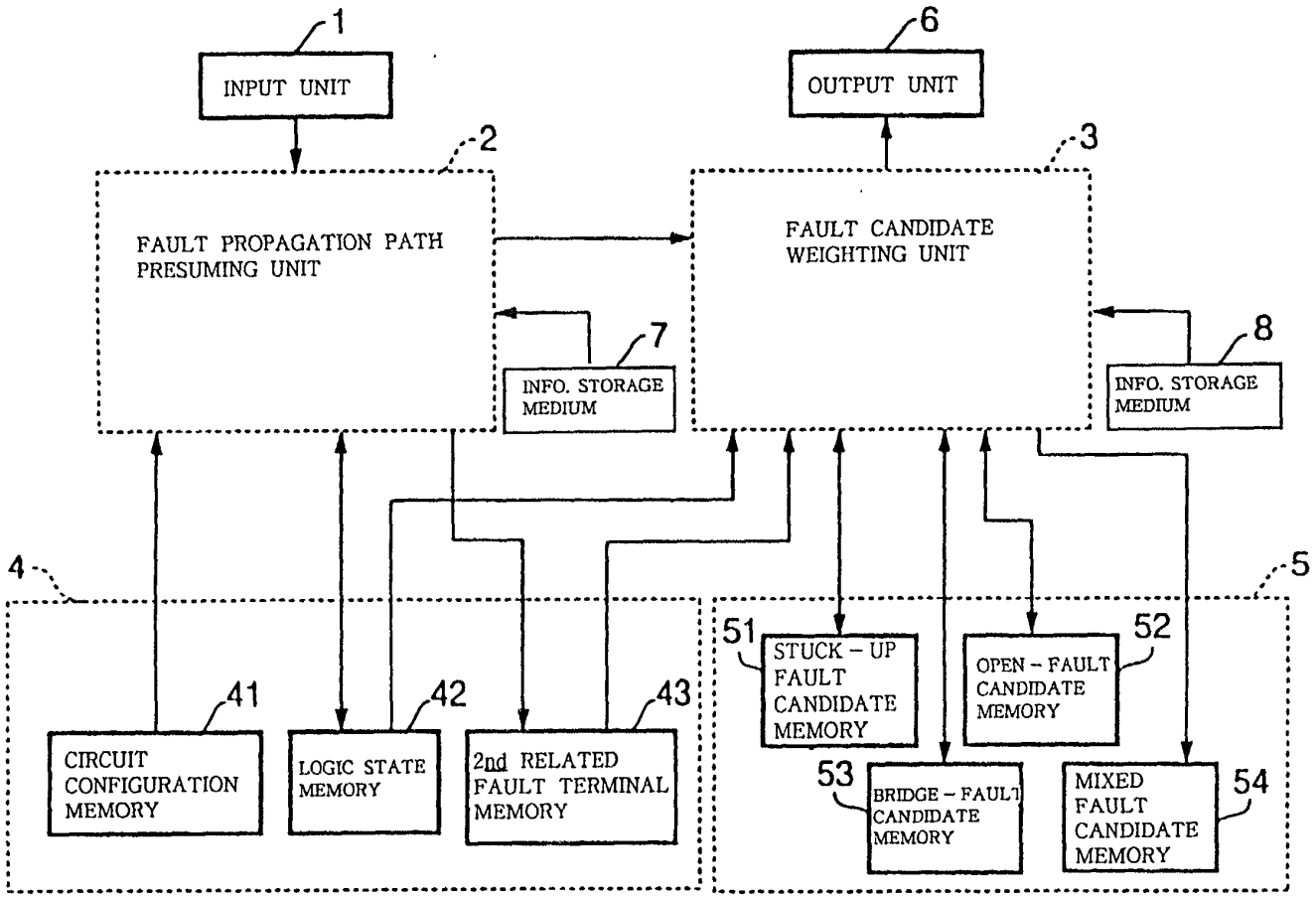
1
INPUT UNIT
6
OUTPUT UNIT
2
FAULT PROPAGATION PATH PRESUMING UNIT
3
FAULT CANDIDATE WEIGHTING UNIT
7
INFO. STORAGE MEDIUM
8
INFO. STORAGE MEDIUM
4
5
41
CIRCUIT CONFIGURATION MEMORY
42
LOGIC STATE MEMORY
43
2nd RELATED FAULT TERMINAL MEMORY
51
STUCK – UP FAULT CANDIDATE MEMORY
52
OPEN – FAULT CANDIDATE MEMORY
53
BRIDGE – FAULT CANDIDATE MEMORY
54
MIXED FAULT CANDIDATE MEMORY

Fig. 23